7 Gbit/s optical JK flip flop design with two optical AND gates and NOR gates*

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This study presents a simple methodology for implementation of all optical JK flip flop for future optical high speed networks. The scheme utilizes electronic model of JK flip flop for implementation of all optical JK flip flop at the bit rate of 7 Gbit/s. Firstly, all-optical AND and NOR gates are implemented. Furthermore, with the combination of these basic gate structures, the optical model of JK flip flop is verified. This structure makes use of two optical AND gates and two optical NOR gates. This technique uses a semiconductor optical amplifier (SOA) as the nonlinear medium to produce considerable amount of cross gain and cross phase modulation to attain truth table conditions of optical JK flip flop. In this method, the number of gates is reduced as compared to earlier schemes. Rise time and fall time of 5.6 ps with contrast ratio more than 60 dB are achieved in this design.

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With increasing interest and existing limitations, the requirement arises for the high speed photonic digital processing to carry out a variety of computational functionalities, such as multiplexing, demultiplexing bit conversations, packet buffering, and header processing, retiming and switching. All these functionalities can be implemented easily at high speed in the optical level without even converting them to electronic domain. This is the main striking feature behind this technology[1]. The main idea of optical implementation of various functionalities is to make the optical system flexible and scalable for the future era[2]. In recent decades, all optical processing has emerged as a promising technology. Over the past several years, a versatile method based on modification of refractive index and gain of semiconductor optical amplifier (SOA) is used to obtain logic functions. The challenging issues behind this are to expand the structure and function of the design and to minimize its complexity. Further, optical delay and feedback are introduced to tackle inherent limitations of problem[3]. In the present era of computing, there is wide advancement in the processor speed, while the memory elements like electronic latches and flip-flops still suffer from narrow bandwidth and protracted access, results in limiting the operation of processor. It is very important to fulfill the gap in between the slow memory devices and high-speed processors. Recent research is centered on designing ultra-high speed optical latching devices and ultra-fast optical memories which are able to provide wide bandwidth at ultra-high bit rates[4]. Numbers of devices have already been explored with the phenomenon of optical bi-stability. The same phenomenon is utilized in Master-slave flip-flop to provide the switching and buffering capabilities based on two lasers connected in ring like structure[5]. Numbers of designs are also based on semiconductor optical amplifier- Mach-Zehnder interferometer (SOA-MZI)[6-9]. Other techniques are also explored which are based on the change in the feedback signal in the case of distributed feedback (DFB) lasers and vertical cylindrical surface radiating lasers[10]. Solutions are also reported based on the properties of erbium doped fibers[11]. Devices require high input control power for operation and result in sluggish switching response reduced contrast value is achieved with transition time in the picosecond level[12,13]. Additionally, good contrast value is attained on the expense of nanosecond-level transition time[14]. There is tradeoff between contrast ratio and operational speed. Optical flip flops based on above techniques suffer from slow transition from one stable state to another due to sluggish rise and fall time in the range of nanoseconds. In this study, a solution is proposed for ultra-high speed JK flip flop with transition time of 5.66 ps for both rising edge and falling time with contract ratio of more than 60 dB. This overcomes the limitation of slow rising and falling edge. In this study, we explore a new unified method. This method is based on nonlinear characteristics of SOA to build basic photonic logic functionalities[15]. In addition to this, a scheme has been developed to obtain all optical JK flip flop at high bit rate of 7 Gbit/s combining optical gate

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functionalities as a building block. In this study, two NOR gates and two AND gates are combined to formulate JK flip-flop as compare to earlier method which requires four AND gates and two NOR gates for the implementation of optical JK flip flop at the bit rate of 2 Gbit/s[16]. However, using this same technique to realize optical D flip flop requires one optical NOT gate along with four NAND gates, and requires one optical NOT gate, two NAND gates along with two NOR gates for the bit rates of 1 Gbit/s and 2 Gbit/s, respectively[17]. One NOT gate and four NAND gates are required to implement D flip flop using SOA-MZI architecture[18].

Arrangement based on SOA-MZI has been used for realization of all optical AND gate and NOR gates at bit rate of 10 Gbit/s. Obtainable logic gates are combined and simulated at bit rate of 7 Gbit/s with delay components for validation of JK flip flop. The most striking features of this structure are simplicity, stability, small energy requirement, compactness, and ultra-high speed of operation. The universality of SOA method finds increased interest in exploring its nonlinear effects for the construction of digital photonic devices.

Fig.1 shows the diagram of cross gain modulation. Two minimum signals are required for this modulation process. One is the information signal whose wavelength λ_1 is to be varied, while the other is the continuous-wave (CW) signal with wavelength λ_2. The input information signal alters the gain of the SOA, resulting in the change of wavelength of CW signal which is launched in SOA. Thus this information signal is superimposed on the CW signal. The most attracting feature of this technology is that the information wavelength can be altered without changing its area of domain. This technique has been steadily gaining in popularity as SOA gain is dynamic and it results in output change of bit to bit value with input power variation[19].

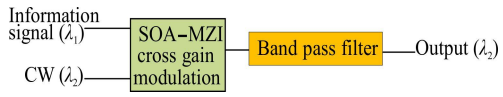

Fig.1 Block diagram of cross gain modulation

This event is based on the phase modification of the resulting wave based on optical power of one more wave. When input signal λ_1 is applied to SOA, the carrier concentration is varied in active state due to depletion in carrier concentration and there is change in refractive index. This changed refractive index influences the change in phase of co-propagating wave λ_2 across the nonlinear device. This process results in cross phase modulation (see Fig.2). This modulation process can overcome the issue related to degradation of extinction ratio[19].

Firstly, the implementation of all optical logic functionalities AND and NOR using the nonlinear properties of SOA in SOA-MZI structure at ultra-high speed of 10 Gbit/s is performed. Secondly, all optical JK flip flop based on basic electronic setup is verified at bit rate of 7 Gbit/s using these obtainable all AND and NOR optical logic functionalities. The SOA is considered as a nonlinear medium. Raising its input power results in reduction of its carrier density, and thus the amplification gain is decreased. This is a very fast course at picosecond-level, which takes place in the carrier concentration of the SOA. This process has a great potential and can be used for alteration of bit to bit value with change in the input power. The SOA-MZI structure is considered in such a way that the optical signals of two SOAs obstruct either additive or subtractive at the output of the interferometer. The additive or subtractive obstruction takes place, which relies on the cosine angle among the optical signals from the sole SOA.

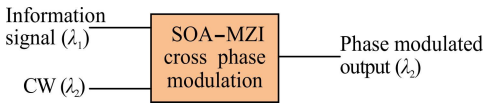

Fig.2 Block diagram of cross phase modulation

The output of AND gate is at “High” logic if the applied inputs are high, otherwise vice versa[20]. The truth table of AND gate is shown in Tab.1. The AND gate is simulated with the help of SOA-MZI utilizing cross gain and cross phase phenomena at bit rate of 10 Gbit/s using input binary sequence taken as 0011 and 0101.

In this scheme, the input binary signal is generated with the help of Gaussian generator as shown in Fig.3. The input signal is provided to one of the inputs of the first SOA with a wavelength of 1 545 nm and power of 0.3 mW with the help of wavelength division multiplexing (WDM) multiplexer. The other input of multiplexer is coupled with the control signal with a wavelength of 1 545 nm and 0.3 mW power. The CW signal with a wavelength of 1 540 nm and 0.25 mW power is coupled to the second SOA. Outputs of two SOAs are coupled and provided to the optical receiver with a bandwidth of 20 GHz and wavelength of 1 540 nm. The output signal is further applied to the non-return-to-zero (NRZ) pulse generator. The resulting output signal is 0001 as shown in Fig.6, which is AND output of two applied data signals of 0011 and 0101[21].

Tab.1 Truth table for AND gate

Input A	Input B	Output
Low	Low	Low
Low	High	Low
High	Low	Low
High	High	High

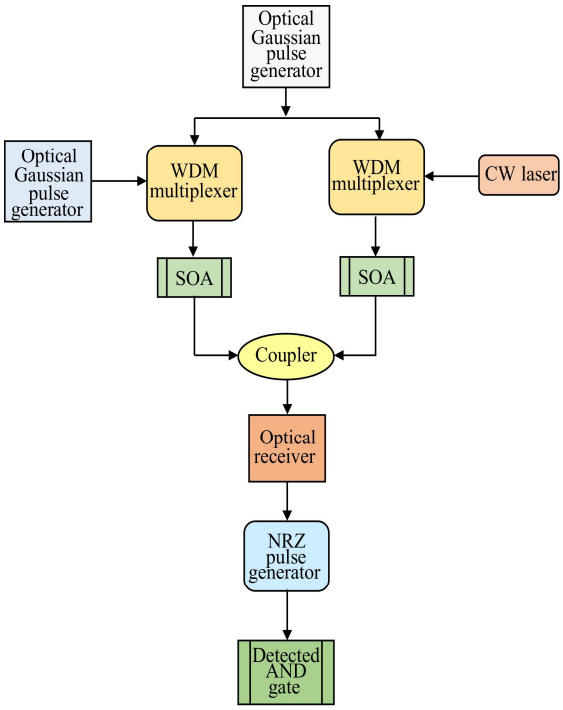

Fig.3 Simulation block diagram of AND gate at 10 Gbit/s

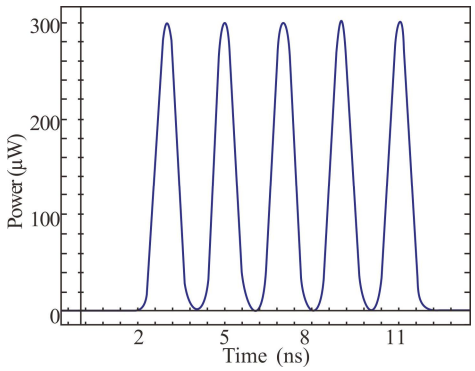

Fig.4 Input A of 0011 to AND gate

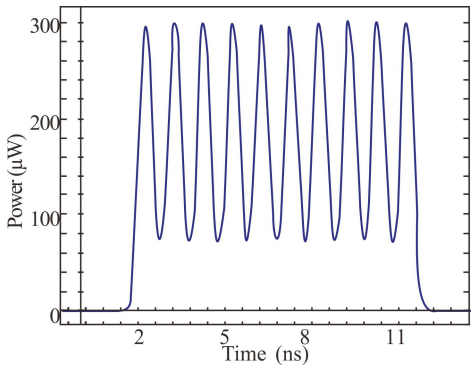

Fig.5 Input B of 0101 to AND gate

The NOR gate output is high only if both inputs are low. The SOA-MZI scheme is used for implementation of this gate. The truth table of NOR gate is shown in Tab.2. The NOR gate is simulated with the help of SOA-MZI utilizing cross gain and cross phase phenomena at bit rate of 10 Gbit/s.

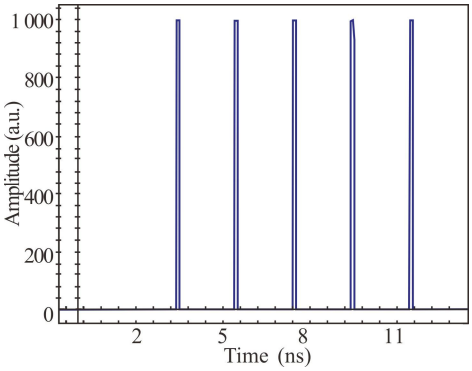

Fig.6 Output 0001 of AND gate at 10 Gbit/s

Tab.2 Truth table for NOR gate

Input A	Input B	Output
Low	Low	High
Low	Low	Low
High	Low	Low
High	High	Low

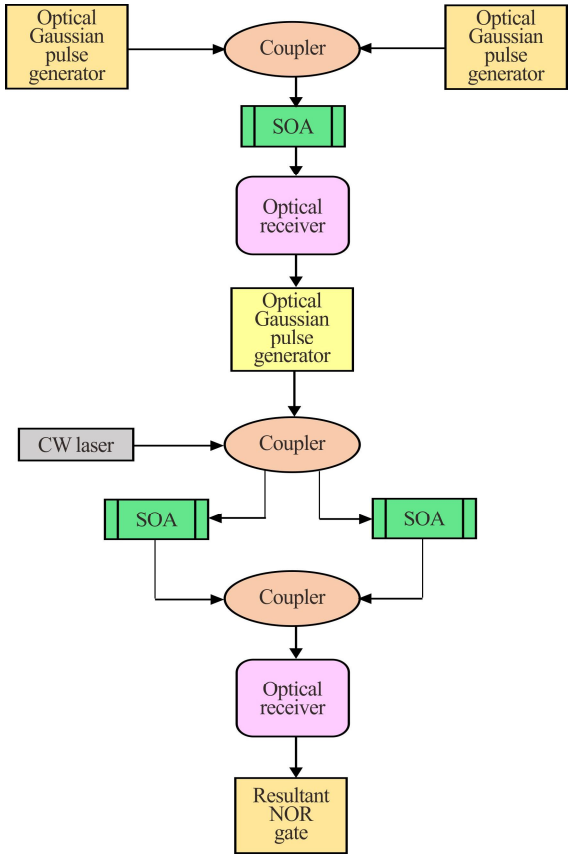

Fig.7 Simulation block diagram of all-optical NOR gate

In this scheme, two data sequences are generated using an optical Gaussian pulse generator at the same wavelength

of 1 545 nm and 0.3 mW power. The first data sequence is taken as 0011, while the second is taken as 0101 to provide inputs for the NOR gate. These signals are coupled and transmitted through the SOA. The received signal is coupled with the continuous control signal with a wavelength of 1 540 nm and 0.3 mW power. The signal is further transmitted to the SOA-MZI structure to produce necessary cross gain and phase modulation effect. The output signal obtained is 1000, which is an NOR output of two input signals of 0011 and 0101[22].

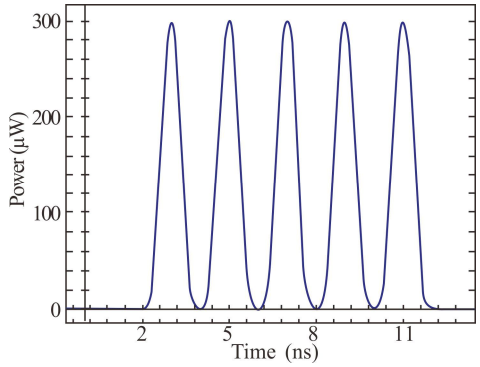

Fig.8 Input A of 0011 to all-optical NOR gate

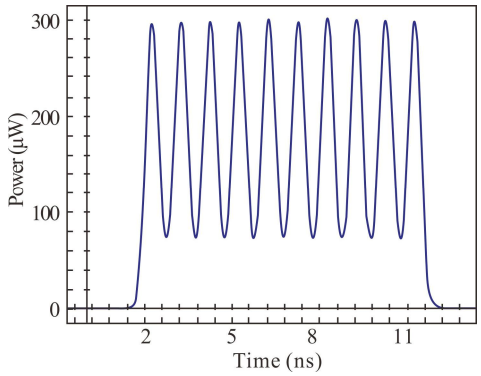

Fig.9 Input B of 0101 to all-optical NOR gate

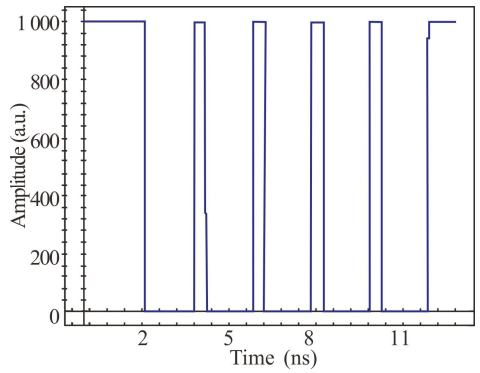

Fig.10 Output 1000 of all-optical NOR gate at 10 Gbit/s

In the design of optical systems, the flip flops are essential components. Among all flip flops, the universality of JK type flip flop makes it very attractive. The structure of JK flip flop with two AND gates and NOR gates is shown in Fig.11.

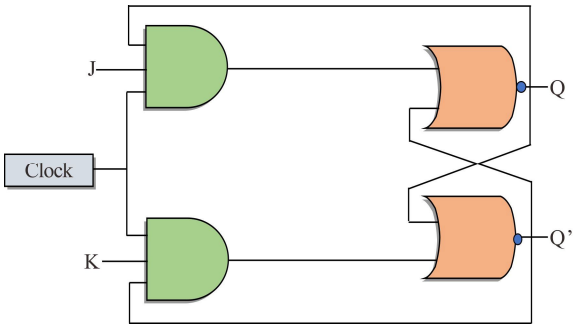

Fig.11 Block diagram of JK flip flop

The JK flip flop has advantages when both inputs are at high logic output toggles[23]. In the toggle state, both outputs of flip flop will change their present values with their reverse values. Output of JK flip flop remains the previous values stored, if both inputs J and K are set at zero. The value of J is stored at output Q_{n+1} in the next clock cycle, if clock is high irrespective of the previous value stored[24]. When output is high, this state is called set state of flip flop, and when output is low, the flip flop is called to be reset as shown in Tab.3.

Tab.3 Truth table for JK flip flop

Clock	Input		Present state		Next state	
	J	K	Q_n	$\overline{Q}_n$	Q_{n+1}	$\overline{Q}_{n+1}$
1	0	0	0	1	0	1
1			1	0	1	0
1	0	1	0	1	0	1
1			1	0	0	1
1	1	0	0	1	1	0
1			1	0	1	0
1	1	1	0	1	1	0
1			1	0	0	1

JK flip flop is implemented at bit rate of 7 Gbit/s with the help of two AND gates and NOR gates as shown in Fig.11. Considerable amount of cross gain and cross phase modulation is optimized inside SOA-MZI for the realization of both AND and NOR gates using the simulation parameters listed in Tab.4.

JK inputs are provided with data signal at a wavelength of 1 545 nm and 0.3 mW power. In this setup, the feedback signal is taken from Q to upper AND gate with optical delay of 100 ps. For the lower AND gate, the feedback signal is taken from $\overline{Q}$ and the optical delay is taken to be 1 ps. The optical delay taken for upper NOR gate from $\overline{Q}$ and for lower NOR gate from Q is taken to be 1 ps. Feedback signal from Q is provided as one of the input to the first AND gate along with clock signal and J inputs. Similarly, feedback signal $\overline{Q}$ along with clock and K input are provided to the next AND gate as shown in Fig.12.

Tab.4 Simulation parameters of AND and NOR gates

Simulation parameter at 7 Gbit/s	AND gate	NOR gate
Bias current (A)	0.14	0.15
Length (μm)	0.000 5	0.000 4
Width (μm)	3×10^{-6}	3×10^{-6}
Height (μm)	8×10^{-8}	8×10^{-8}
Initial carrier density	3×10^{23}	3×10^{23}
Differential gain (m^{-3})	27.8×10^{-21}	27.8×10^{-21}
Optical confinement factor	0.3	0.3
Line width enhancement factor	5	5
Carrier density at transparency	1.4×10^{24}	1.4×10^{24}
Recombination coefficient A (s^{-1})	1.43×10^{8}	1.43×10^{8}

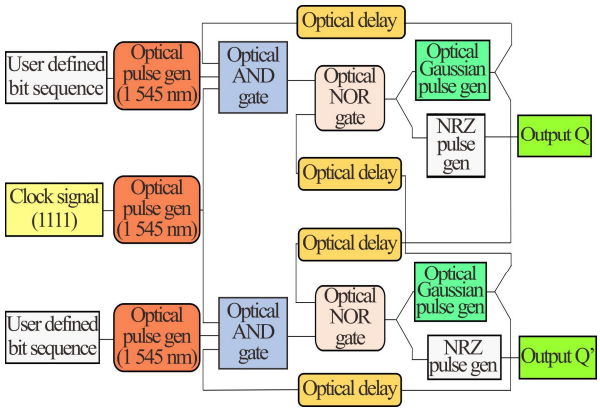

Fig.12 Block diagram of all optical JK flip flop

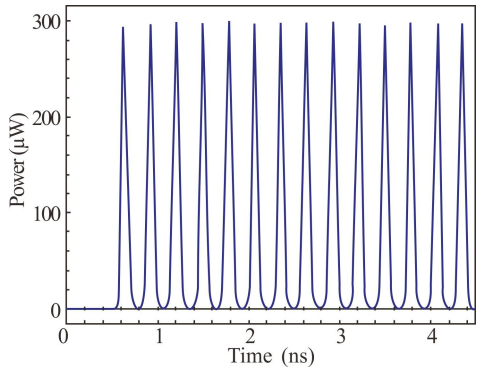

Fig.13 Input J of JK flip flop 0101

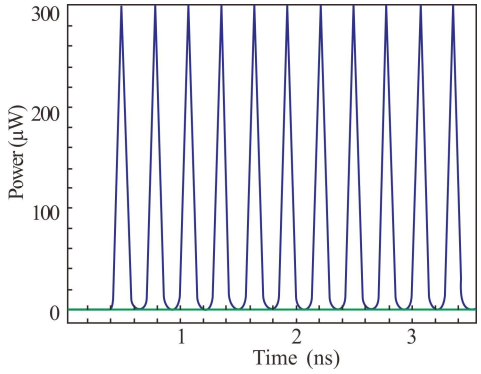

Fig.14 Input K of JK flip flop 1010

Two user defined sequences of 0101 and 1010 are applied at the wavelength of 1 545 nm with predefined clock signal as high as 1111 at ultra-high bit rate of 7 Gbit/s[16]. When the value of J is low and K is at high logic, the output will reset (Q_{n+1}=0 and $\bar{Q}_{n+1}$=1) irrespective of previous values stored. When J is set high and K is low, flip flop settles in opposite state. The Q_{n+1} represents the output state of JK flip flop, Q_n represents the previous state, while JK are the applied inputs to the optical JK flip flop. Based upon Tab.5, the state equation and Fig.16 can be obtained.

Tab.5 Characteristic table for JK flip flop

Input			Output	
Q_n	J	K	Q_{n+1}	Q'_{n+1}
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

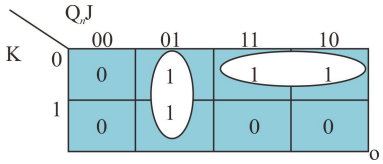

Fig.15 The K map

$$Q_{n+1} = \bar{Q}_n J + Q_n \bar{K}. \quad (1)$$

JK flip flop has two stable states of 0 and 1. When the present state of JK flip flop is 0, input J=1, and K=X (it can be 0 or 1), there is a state transition to state 1. On the other hand, if the JK flip flop is in state 1, input J=X (it can be 0 or 1), and K=1, there will be transition to state 0. This transition 0101 is achieved in optical flip flop for applied J input of 0101 and K input of 1010.

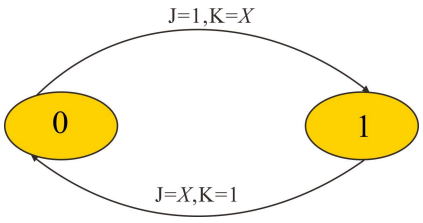

Fig.16 State diagram of optical flip flop at 7 Gbit/s

In this design, the output of 0101 is obtained for Q_{n+1} when clock is high to enable input signals. Signal J is set at high while K is set at low value, which will make the output Q_{n+1} irrespective of the previous state. Similarly, the output of optical flip flop will reset irrespective of the last state when J is set at low value and K is set at high value. In other words, output state Q will store the

value of J in the next clock. Speed is directly proportional to time taken by the flip flop to change from low to high or high to low state. In the high speed optical processing networks, a large number of flip flops are employed. The increase of rise time and fall time will make the system slow and sluggish.

The speed of flip flop depends on the rise time and fall time[25]. Rise time and fall time should be matched. Rise time and fall time of JK flip flop is a time span to adjust state from 0 to 1 or from 1 to 0, and is measured at 10% and 90% points, respectively. In this study, rise time and fall time is measured to be 5.66 ps. This implies more rapid speed in case of optical memory as compared to electronic RAM operation which is measured in nanosecond level. Further, contrast ratio of 60 dB is achieved at 7 Gbit/s.

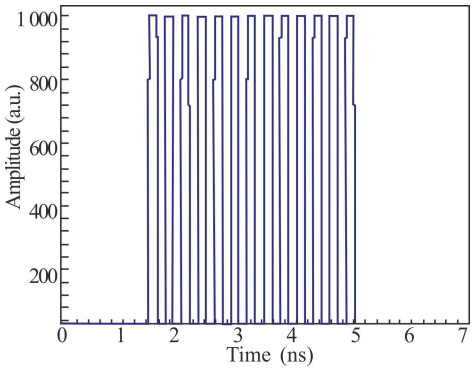

Fig.17 Output for Q_{n+1} of JK flip flop 0101

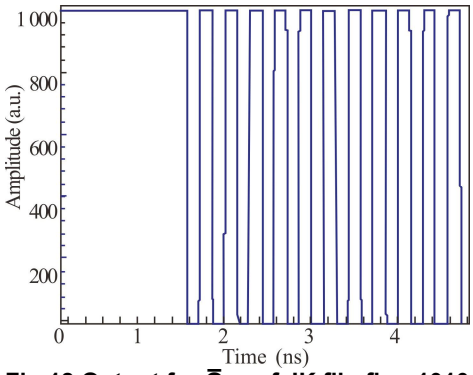

Fig.18 Output for $\overline{Q}_{n+1}$ of JK flip flop 1010

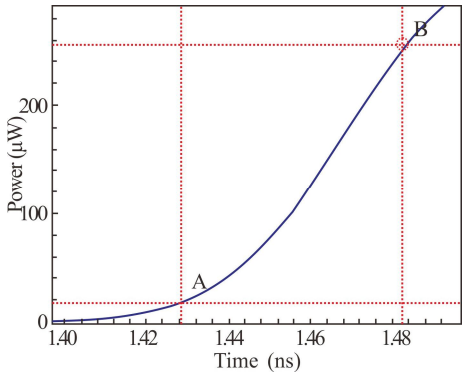

Fig.19 Rise time to be 5.66 ps

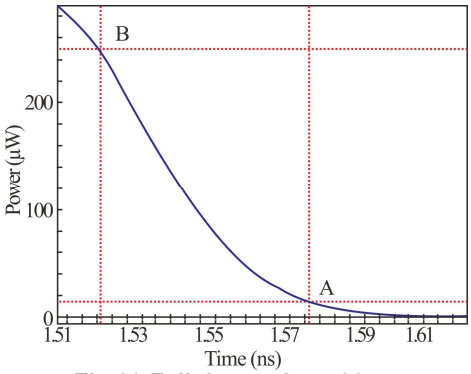

Fig.20 Fall time to be 5.66 ps

A simple technique is used to investigate all optical JK flip flop based on electronic model consisting of two optical AND gates and two NOR gates. Speed is improved to a large extend due to small rise time and fall time of 5.66 ps. The number of gates is reduced in this design as compared to earlier schemes. The realized flip flop has an integrated structure with high transition speed and consumes less power at bit rate of 7 Gbit/s.

Statements and Declarations

The authors declare that there are no conflicts of interest related to this article.

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