Ultra-low dark count InGaAs/InP single photon avalanche diode*

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A low noise InGaAs/InP single photon avalanche diode (SPAD) is demonstrated. The device is based on planar type separate absorption, grading, charge and multiplication structure. Relying on reasonably designed device structure and low-damage Zn diffusion technology, excellent low-noise performance is achieved. Due to its importance, the physical mechanism of dark count is analyzed through performance characterization at different temperatures. The device can achieve 20% single photon detection efficiency and 320 Hz dark count rate (*DCR*) with a low after pulsing probability of 0.57% at 233 K.

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InGaAs/InP single photon avalanche photodiode (SPAD) has the advantages of good performance, low cost, small size, and no need for ultra-low temperature cooling. It is the mainstream technical solution and mainstream technology development direction for single-photon detection in the near-infrared band[1]. It is widely applied to the fields of quantum communication and quantum information[2], laser detection and laser imaging[3,4], molecular luminescence and quantum spectroscopy analysis[5]. Especially with the rapid development of quantum secure communication, InGaAs/InP SPAD has become a research and development hotspot[6]. The planar InP-based separate absorption, grading, charge and multiplication (SAGCM) structure is widely adopted in this application due to its high reliability, low noise, high quantum efficiency and high gain-bandwidth product[7]. In recent years, with the development of material quality and chip structure, the performance of InGaAs/InP SPAD has been greatly improved. It can reach 20% photon detection efficiency (*PDE*) at a wavelength of 1.55 μm and 1 kHz level dark count rate (*DCR*) at 223—233 K[8,9]. However, the application requirements for its performance are still improving. Thus, the development of higher performance devices is of great significance.

Two main types of noises exist in SPAD, dark count (DC) and after pulsing (AP) noises. *DCR* is the total DC in 1 s, and after pulsing probability (*APP*) is the ratio of after pulsing count to photon count. DC is the intrinsic noise of SPAD, which limits device performance in all application scenarios, while AP becomes important only in high frequency application scenarios. Thus, understanding the physical mechanism and analyzing the source of DC is important for the development of high-performance devices.

An ultra-low-noise bottom-illuminated planar structure InGaAs/InP SPAD is demonstrated in this letter. The epitaxial structure which is grown by metal-organic chemical vapor phase deposition (MOCVD) on n-InP substrate is shown in Fig.1. It consists of an n-InP buffer layer, an unintentionally doped InGaAs absorption layer, three unintentionally doped InGaAsP grading layers, an Si doped InP charge layer, and an unintentionally doped InP cap layer. The grading layers are used to prevent hole piling up at the heterointerface between absorption layer and charge layer.

Low-damage Zn diffusion technology is used to form a stepped structure, which can gradually weaken the edge electric field intensity. Thus edge breakdown is restrained. The Zn diffusion depth d can be expressed as a function of diffusion time t as

$$d = A\times\sqrt{t}, \tag{1}$$

where A is a function of the diffusion condition and material. Different Zn diffusion depths can be obtained by fixing the diffusion condition and changing the diffusion time. In this letter, the thickness of the multiplication layer is controlled to be about 1 μm. In the center region, Zn diffuses deeper than in the peripheral region. In this condition, the electric field of the periphery region is lower than the center region, and thus edge breakdown is restrained.

The chips are packaged into a coaxial structure with a pigtail to receive the single photon optical signal. Then, the performance is measured at different temperatures and different voltages.

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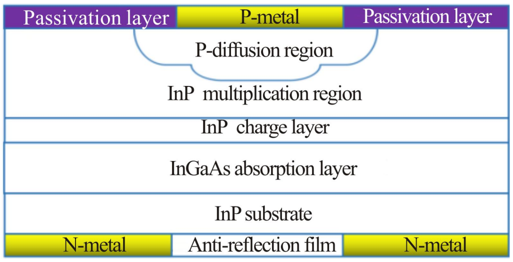

Fig.1 Schematic diagram of planar type InGaAs/InP SPAD

The Geiger mode performance of the coaxial-packaged device is measured. The test gate frequency f_g is 1 MHz with a gate voltage V_g of 6 V and gate width t_g of 4.4 ns, the optical pulse frequency f_{ph} is 100 kHz with average photon per pulse μ=1, the test time t is 60 s, and the optical wavelength λ is 1.55 μm. The *PDE*, *DCR* and *APP* are calculated as follows

$$PDE = \frac{1}{\mu}\ln\frac{1-R_{d}/(f_{g}\times t)}{1-R_{ph}/(f_{ph}\times t)}, \tag{2}$$

$$DCR = \frac{R_{d}}{f_{g}\times t_{w}\times t}, \tag{3}$$

$$APP = \frac{R_{a}-0.9\times R_{d}}{R_{ph}}, \tag{4}$$

where R_d is the measured counts with laser off, R_{ph} is the measured counts at the gates with photon signal, R_a is the measured counts at the 9 gates after photon signal as shown in Fig.2, and t_w is the effective gate width. Through changing the delay between the photon signal and the gate and measuring the photon counts, t_w is measured as full width at half maximum (*FWHM*) of the photon counts, as shown in Fig.3. The typical value of t_w is 1 000—3 000 ps depending on the bias voltage, which is slightly smaller than t_g.

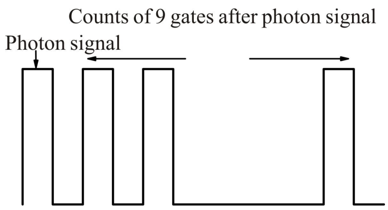

Fig.2 Diagrammatic sketch of *APP* test

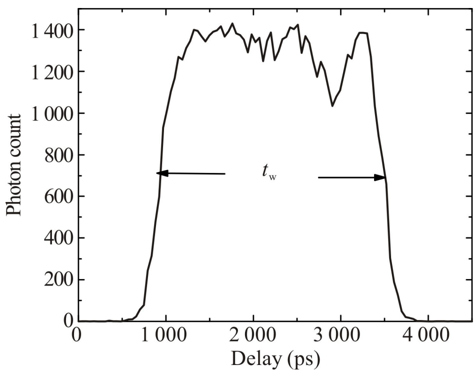

Fig.3 Diagrammatic sketch of effective gate width

Fig.4 and Fig.5 show the typical *DCR* and *APP* characteristics as a function of *PDE* of a device at 233 K. *DCR* is caused by dark carriers without photon signal, which is the basic noise of the device. Thus, analyzing its generation mechanism is beneficial to research high performance chips. *APP* is caused by trapping and releasing carriers generated by avalanche process in the multiplication, and it is important in high frequency application scenarios. The highest *PDE* is 32.6%, which is limited by the low gate voltage. The *DCR* and *APP* increase faster than *PDE*, which means that the device performance cannot be improved by indefinitely increasing the bias voltage.

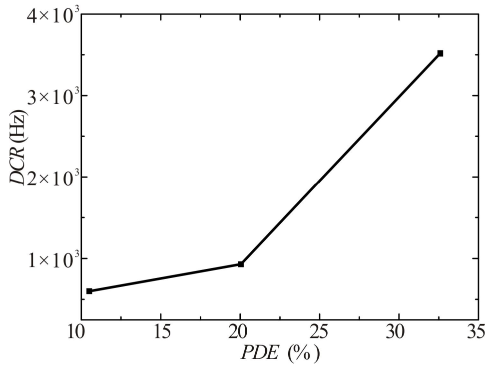

Fig.4 *DCR* as a function of *PDE*

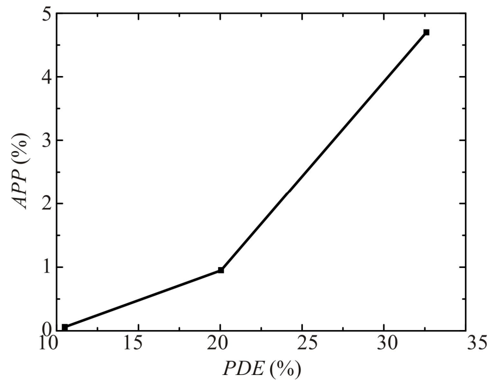

Fig.5 *APP* as a function of *PDE*

Fig.6 shows the typical *DCR*-temperature characteristics of a device at a *PDE* of 20%. The *DCR* increases exponentially with temperature for about one order of magnitude every 30°.

DCR can be caused by dark carriers generated through tunneling in the multiplication region or Shockley-Read-Hall (SRH) in the absorption region.

Dark carriers generated through SRH in the absorption region is expressed as

$$N_{SRH} = \frac{n_{i}}{\tau_{SRH}}, \tag{5}$$

where τ_{SRH} is the carrier lifetime, and n_i is the intrinsic carrier concentration which is expressed as

$$n_{i} = \sqrt{N_{C}\times N_{V}}\times\exp(-\frac{E_{g}}{2\times k\times T}), \tag{6}$$

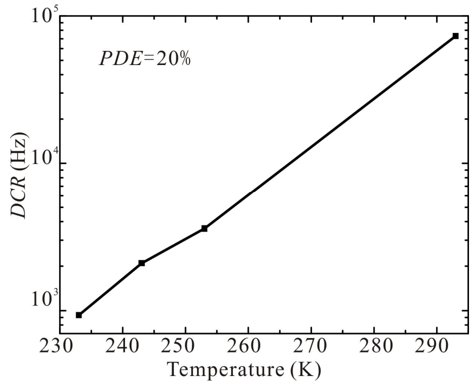

Fig.6 *DCR* as a function of operating temperature

where E_g is the material band gap energy, N_C and N_V are the effective density of states of the conduction band and the valence band, respectively, k is the Boltzmann's constant, and T is the temperature of the lattice. N_C and N_V are proportional to $T^{1.5}$, the scale factor is set to be $38.5/(\mu m^3 \cdot K^{1.5})$ for N_C and $1\,600/(\mu m^3 \cdot K^{1.5})$ for N_V while the accuracy of the scale factor does not affect the conclusion. For InGaAs, E_g is a function of temperature as[10]

$$E_g = 0.819 - (\frac{2.73 \times 10^{-4}}{T+300} + \frac{2.22 \times 10^{-4}}{T+271}) \times T^2. \tag{7}$$

The calculated n_i as a function of temperature is plotted in Fig.7. As can be seen, n_i increases about one order of magnitude every 30°, which agrees well with *DCR*-temperature characteristic of the device. In fact, when the carrier lifetime is set to 90—1 600 μs, the simulation *DCR* result is in good agreement with the test *DCR* result.

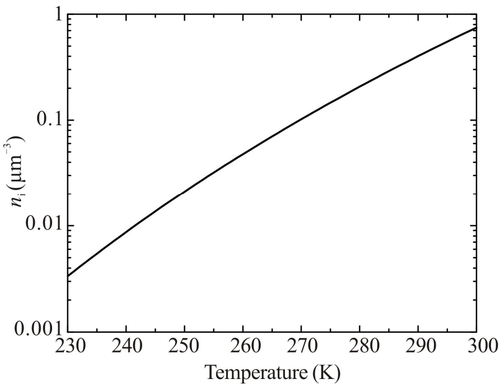

Fig.7 Intrinsic carrier concentration as a function of temperature of the absorption layer

The dark carriergeneration rate per unit volume through band-to-band tunneling is expressed as Eq.(8), and that through trap assisted tunneling is expressed as Eq.(9):

$$N_{\mathrm{bbt}} = \frac{\sqrt{2m_r}\, q^2 E^2}{4\pi^3 \hbar^2 \sqrt{E_g}} \exp(-\frac{\pi \sqrt{m_r} E_g^{3/2}}{2\sqrt{2} qE\hbar}), \tag{8}$$

$$N_{\mathrm{TAT}} = \frac{\sqrt{\frac{2m_r}{E_g}} \frac{q^2 E^2}{4\pi^3 \hbar^2} N_{\mathrm{Trap}} \exp(-\frac{\pi\sqrt{m_{\mathrm{lh}} E_{\mathrm{B1}}^3} + \pi\sqrt{m_e E_{\mathrm{B2}}^3}}{2\sqrt{2} q\hbar E})}{N_V \exp(-\frac{\pi\sqrt{m_{\mathrm{lh}} E_{\mathrm{B1}}^3}}{2\sqrt{2} q\hbar E}) + N_C \exp(-\frac{\pi\sqrt{m_e E_{\mathrm{B2}}^3}}{2\sqrt{2} q\hbar E})}, \tag{9}$$

where E is the electric field intensity, $m_e = 0.08m_0$ is the effective electron mass, m_0 is the free-electron mass, $m_{\mathrm{lh}} = 0.089m_0$ is the effective light-hole mass, N_{Trap} is the trap concentration, and E_{B1} and E_{B2} are the barrier heights from the valence band to the trap and from the trap to the conduction band, respectively. According to the research results of MCINTOSH et al[11], for InP, $E_{\mathrm{B1}} = 0.75E_g$ and $E_{\mathrm{B2}} = 0.25E_g$. Carrier reduced effective mass m_r is expressed as

$$m_r = \frac{2m_e * m_{\mathrm{lh}}}{m_e + m_{\mathrm{lh}}}. \tag{10}$$

For a multiplication region width of about 1 μm, dark carriers generated through tunneling increase about 20 times while the temperature increases from 220 K to 300 K[12], which is much slower than *DCR*.

Thus, *DCR* is meanly caused by dark carriers generated through SRH in the absorption region.

Fig.8 shows the typical *APP*-temperature characteristics of a device. The *APP* decreases with temperature, which means that the lifetime of the trapped carriers decreases with temperature.

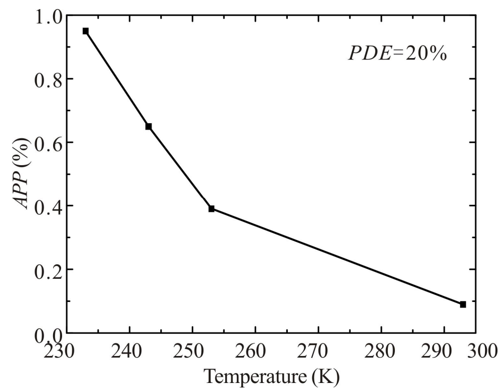

Fig.8 *APP* as a function of temperature

Fig.9 shows the *DCR* and *APP* characteristics of 17 devices at 233 K. The *PDE* is 20%. As can be seen, the lowest *DCR* is 320 Hz with *APP* of 0.57% at the same time, while the lowest *APP* is 0.38% with *DCR* of 360 Hz at the same time. As a contrast, Tab.1 shows some typical recent achievements reported. Such a low noise benefits from high-quality crystal growth, low damage processing and good edge breakdown suppression. At the same time, both *DCR* and *APP* diverse more than one order of magnitude as shown in Fig.9, which may indicate that device performance is strongly dependent on crystal quality and process damage.

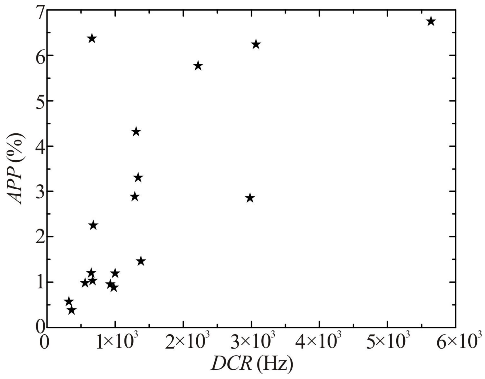

Fig.9 *APP* as a function of *DCR* of 17 devices

Tab.1 Some typical recent results of InGaAs/InP SPAD

DCR (Hz)	*PDE*	Temperature (K)	Year	Institute
950	10	223	2017	University of Science and Technology of China[3]
700	20%	233	2015	Princeton Lightwave Inc.[8]
1 000	25	225	2022	Dipartimento di Elettronica[9]
~1 000	20%	233	2021	Wooriro Co., Ltd.[13]
~4 100	10%	243	2019	University of Shanghai for Science and Technology[14]
4 100	21%	223	2021	Institute of Semiconductors, Chinese Academy of Sciences[15]
320	20%	233	-	This work

In summary, we have demonstrated a planar structure InGaAs/InP SPAD which is fabricated by Zn diffusion. At 233 K and *PDE* of 20%, the *DCR* can be as low as 320 Hz, and the *APP* can be as low as 0.57% at the same time.

Statements and Declarations

The authors declare that there are no conflicts of interest related to this article.

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