A high dynamic range pixel using lateral overflow integration capacitor and adaptive feedback structure in CMOS image sensors*

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This letter proposes a novel high dynamic range (*HDR*) pixel using lateral overflow integration capacitor (LOFIC) and adaptive feedback structure. Through detailed analysis of the voltage feedback mechanism, the conversion gain (*CG*), full well capacity (*FWC*) and dynamic range (*DR*) performances of the feedback LOFIC pixel are analytically expressed. The verification results reveal that the equivalent *FWC* of the feedback LOFIC pixel is 1.89 times of conventional LOFIC pixel, and the *DR* extension is 5.5 dB. Based on 110 nm CMOS process, a 5.0 μm pixel layout is presented, using 13.3 fF capacitance to achieve 83 ke- *FWC* and 102.8 dB *DR*, which are 44 ke- and 97.3 dB of conventional LOFIC pixel under the same design conditions. This also demonstrates that the feedback LOFIC pixel can reduce the dependence of extended *DR* on capacitor area, and can be used as a reference for *HDR* pixels design.

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CMOS image sensors (CISs) play a significant role in sensing applications, such as healthcare, machine vision and aerospace[1]. To improve the sensing ability of image information, high dynamic range (*HDR*) CISs are widely required[2,3]. The dynamic range (*DR*) mainly depends on the ability of the photosensitive device to collect photogenerated charge and perform effective charge-voltage conversion. For low light imaging, high conversion gain (*HCG*) and low noise techniques are usually used to achieve high sensitivity image quality[4]. For high light imaging, it is necessary to improve the full well capacity (*FWC*) of pixels and combine low conversion gain (*LCG*) technique to acquire high saturation signals[5]. However, the development of low noise technique is relatively mature, and the level of deep sub-electronic noise can be achieved, almost reaching the limit[6,7]. Therefore, increasing the *FWC* becomes a significant method to extend the *DR*.

The pixels based on lateral overflow integration capacitor (LOFIC) technology also employ the double conversion gain technique[8,9]. But the difference is that LOFIC pixels effectively utilize overflow charge, break through the restriction of charge collection by photodiode (PD), and achieve greater extension of *FWC*. LOFIC pixels are conducive to the detection of high light signals, and can effectively solve the problem of image overexposure by extending the *DR*[10].

The *DR* extension of LOFIC pixels depends on the large capacitor area[11], which is limited in the development trend of chip miniaturization and small pixel pitch. In 2022, OIKAWA et al[12] developed a 120 dB *HDR* LOFIC pixel with a pitch of 22.4 μm. The usual direction of researchers' efforts is to improve the capacitance density, such as the development of MIM, MOM and trench capacitors[12,13]. In 2018, TAKASE et al[11] presented an in-pixel 3D capacitor, which achieved high capacitance density of 41.7 fF/μm^2.

In addition to constantly breaking through the capacitance density by process, it is very necessary to study the method of obtaining high *FWC* and *DR* without a large capacitor. In this letter, a novel LOFIC pixel that combines the adaptive feedback structure is developed. It is beneficial to change the charge-voltage conversion characteristic and reduce the high light conversion gain (*CG*). The feedback LOFIC pixel effectively extends the *FWC* and *DR* performances with reduced capacitance dependence.

The conventional LOFIC pixel structure is shown in Fig.1(a). The pinned photodiode (PPD) accumulates photogenerated charge and the floating diffusion (FD) node is responsible for charge-voltage conversion. A LOFIC is used to collect a large amount of overflow

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charge from PPD under high light[14]. In addition, CSX and CSY nodes represent the bipolar plates of the capacitor. TG is a transfer gate for PPD. SG is a control gate to interconnect FD and CSX nodes. RST is responsible for resetting PPD, FD and CSX nodes. The pixel charge-voltage conversion signals are read out by the source follower (SF) and the row selective transistor (SEL).

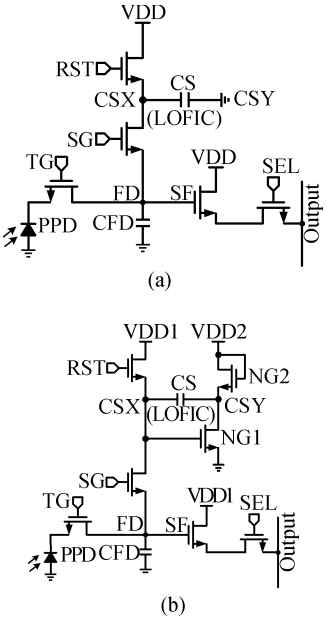


Fig.1 Structure schematic of (a) conventional LOFIC pixel and (b) feedback LOFIC pixel

The feedback LOFIC pixel structure proposed in this letter is shown in Fig.1(b). Compared with the conventional LOFIC pixel, voltage feedback is generated by adding two transistors, NG1 and NG2, to the CSX and CSY nodes. In addition, a power supply VDD2 is added. Fig.2 presents the corresponding feedback loop and common-source amplifier model. NMOS is used as the load to form negative feedback structure of common-source amplifier with gain of A.

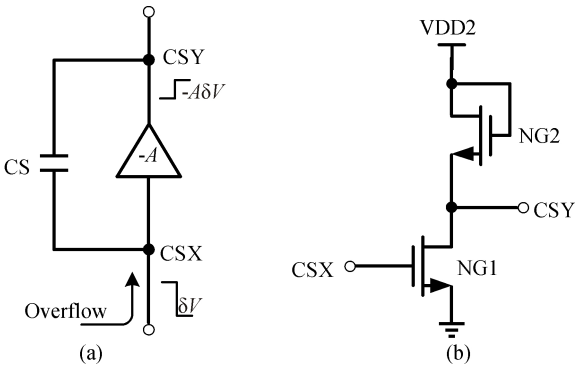


Fig.2 (a) Feedback loop; (b) Common-source amplifier model

The gain parameter A of the common-source amplifier in the feedback loop meets Eq.(1). The parameter A is related to the size of transistors NG1 and NG2, which can be adjusted by designing different W/L ratio. γ is a parameter related to the bulk effect, $\gamma=g_{mb2}/g_{m2}$.

$$A=\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\gamma}. \tag{1}$$

At the same time, the voltage variation at CSX and CSY nodes is also related to voltage coupling coefficient α. When the CSX node generates a voltage drop δV due to the overflow charge, it is input to the feedback structure through the NG1 gate. It leads to the voltage of the CSY node raised by $A\delta V$, and then coupled to the CSX node, the voltage is raised by $\alpha A\delta V$. That is, after a feedback process, the equivalent voltage drop at CSX is $(1-\alpha A)\delta V$, denoted as $\delta V1$, as shown in Eq.(2). Therefore, based on this behavior-level modeling, the feedback process is repeated N times to obtain the equivalent voltage drop δVE at CSX node, as presented in Eq.(3).

$$\delta V1=\delta V-\alpha A\delta V=(1-\alpha A)\delta V, \tag{2}$$

$$\delta VE=\delta V-\alpha A\delta V+\alpha^2A^2\delta V-\alpha^3A^3\delta V+\cdots+\alpha^NA^N\delta V=\frac{\delta V}{1+\alpha A}. \tag{3}$$

Therefore, the voltage variation sensitivity of CSX node decreases, which reduces the CG, and equivalently extends the capacitance. If CS is denoted as the capacitance of LOFIC, and CSE is denoted as the equivalent capacitance value after adding the feedback loop, we get

$$CSE=(1+\alpha A)CS, \tag{4}$$

where α is related to the capacitance composition at CSX node. Considering the capacitance CS and parasitic capacitance CSP, the voltage coupling coefficient α meets $\alpha=CS/(CS+CSP)$.

According to the above analysis, in the feedback structure, the equivalent voltage drop δVE varies with A and α. When the initial voltage drop without feedback is δV=1 V (from 2.8 V to 1.8 V), the voltage feedback process is shown in Fig.3(a). The feedback process can be understood as N times of negative feedback from an initial voltage drop, and finally the node voltage reaches a steady state. To ensure the implementation of voltage drop and negative feedback, the value range of A is preferably between 0 and 1. By changing the value of A, multiple experiments can be set for comparison. Steady-state voltage at different gains A=0.9, 0.7, 0.5 is obtained to characterize the influence of feedback on the node voltage drop. It can be observed that compared with the structure without feedback, the δVE decreases after feedback, and the effect becomes more significant with the increase of A.

In addition, the feedback setting time is worth considering and can be obtained by circuit transient simulation. Fig.3(b) presents the voltage drop when the FD and CSX nodes are connected after the SG transistor is turned on. The transient performances are different for the conventional LOFIC and feedback LOFIC structures. It can be

observed that the voltage without feedback passes 25 ps to be completely stable after experiencing the ultra-transient switching effect of the SG transistor. The voltage drop with feedback will rise and reach stable successfully. Different gains A=0.9, 0.7, 0.5 are further adjusted, and the results show that the setting time of voltage feedback are 75 ps, 100 ps, and 135 ps, respectively. In general, compared with the μs level on-time of SG transistor, the feedback process takes a very short time to establish and does not affect the timing control of pixels.

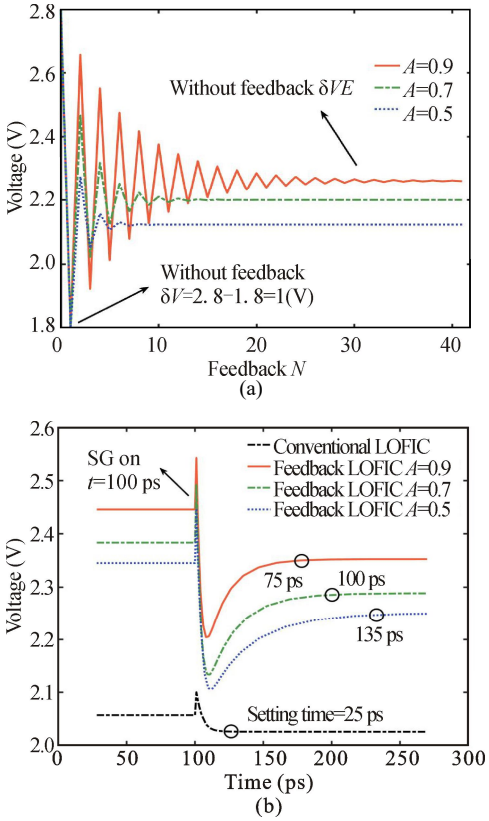


Fig.3 (a) Node voltage feedback with different *A*; (b) Setting time of the conventional and feedback LOFIC pixels when the SG transistor is turned on

The *FWC* and *LCG* of conventional LOFIC pixels are mainly determined by the *CS* capacitor. *LCG* can be directly represented by the voltage variation ΔV caused by the charge variation ΔQ. Therefore, if the swing of pixel output is ΔV_{SW}, *FWC*_LOFIC can be calculated by ΔV_{SW}, and *LCG* as

$$FWC\_\mathrm{LOFIC} = \frac{\Delta V_{SW}}{LCG} = \frac{\Delta V_{SW} \times \Delta Q}{\Delta V}. \tag{5}$$

For the proposed feedback LOFIC pixel, the equivalent *FWC* and *DR* are denoted as *FWC*_LOFIC_E and *DR*_E. According to the above expression of *LCG*, *FWC*_LOFIC and the adaptive voltage adjustment of the feedback structure, *FWC*_LOFIC_E and *DR*_E can be expressed as

$$FWC\_\mathrm{LOFIC\_E} = \frac{\Delta V_{SW} \times \Delta Q}{\Delta VE} = \frac{(1+\alpha A)\Delta V_{SW} \times \Delta Q}{\Delta V}, \tag{6}$$

$$DR\_\mathrm{E} = 20\lg\left(\frac{FWC\_\mathrm{LOFIC\_E}}{\sigma}\right). \tag{7}$$

Therefore, compared with the conventional LOFIC pixel, the feedback LOFIC pixel can effectively extend the *FWC* by $(1+\alpha A)$ times. The value of *DR* is also related to the noise σ.

The *FWC* and *DR* performances are further investigated by device level verification. Fig.4 presents the mixed-mode verification diagram of the feedback LOFIC pixel. According to the device process, the PPD, TG, SG and RST are fabricated on the P-type substrate. The *CS* capacitor and transistors are connected to each node. Conventional and feedback LOFIC pixels can be compared under different designs with or without feedback structure.

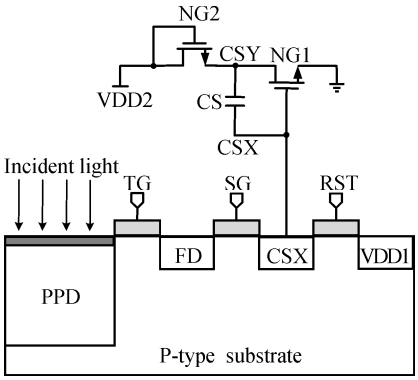
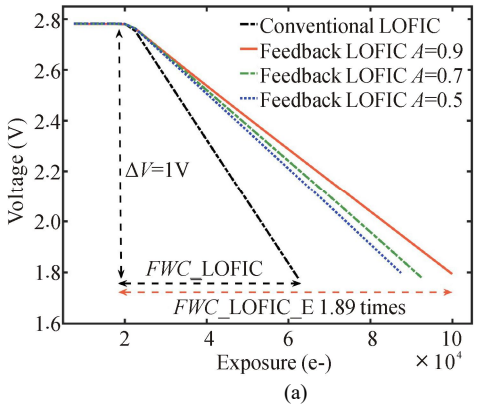


Fig.4 Verification of feedback LOFIC pixel

As the pixel exposure electrons increase, the charge gradually overflows to CSX node, resulting in the voltage decrease. Fig.5(a) presents the electrons number for conventional and feedback LOFIC pixels when the voltage swing is 1 V. It also reveals the full well capacity *FWC*_LOFIC and *FWC*_LOFIC_E. When A=0.9, 0.7 and 0.5 are adjusted, the *FWC*_LOFIC_E are 1.89, 1.69 and 1.49 times that of *FWC*_LOFIC. The results demonstrate that due to the addition of feedback structure, the voltage drop becomes insensitive and the extension of *FWC* is achieved.



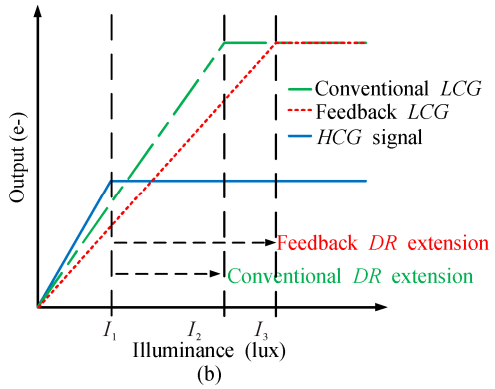


Fig.5 (a) *FWC* extension with *A*=0.9, 0.7 and 0.5 during exposure; (b) *DR* extension schematic diagram

Fig.5(b) is a schematic diagram of the pixel *DR*, which is illustrated with different *CG*. Based on the *HCG* signal obtained by PPD, the conventional LOFIC pixel uses capacitive *LCG* signal to achieve the *DR* extension. The *FWC* and *DR* of the proposed feedback LOFIC pixel are further extended by reducing the conversion gain.

The *DR* of pixels can be calculated by *FWC* and the noise σ, as presented in Eq.(7). σ represents the minimum noise level, corresponding to the low light signal. For the proposed feedback LOFIC pixel, the FD node is used to read the low light signal. This is the same as the conventional LOFIC pixel, so the σ is basically the same. Based on the *FWC* extension of 1.89 times, when the design value of σ fluctuates between 0.2 e- and 1.2 e-, the corresponding *DR* changes as shown in Fig.6. The σ affects the value of *DR*, and the smaller the σ, the larger the *DR*. However, compared with the conventional LOFIC pixel, the relative amount of *DR* extension of the feedback LOFIC pixel is 5.5 dB. In addition, many techniques have been proposed to reduce σ to deep sub-electronic noise level, such as correlated multiple sampling technique by readout circuit designing[6,15]. In the following research, σ uses 0.6 e- as a reference value to calculate the *DR*.

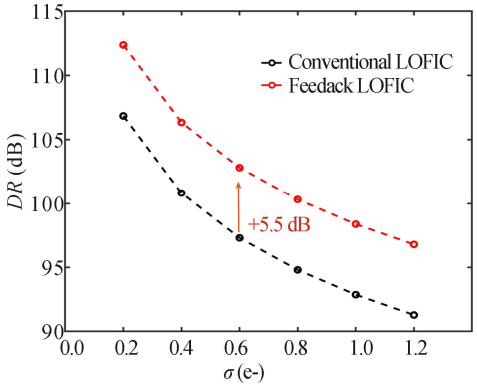


Fig.6 Dynamic ranges of the conventional and feedback LOFIC pixels under different noise values

For the proposed feedback LOFIC pixel, due to the addition of supply voltage VDD2 and the branch, it is necessary to study its operating current. Based on obtaining the operating current curves, the average current in the whole operating timing can be calculated, as shown in Fig.7(a). Adjusting VDD2=3.3 V, 2.5 V and 1.8 V while ensuring that transistor NG1 operates in the saturation region. The results reveal that average operating current is 1.77 μA, 1.16 μA and 0.60 μA, respectively. In theory, as the supply voltage VDD2 decreases, the drain voltage of NG1 will decrease, which will indeed result in a decrease of the current.

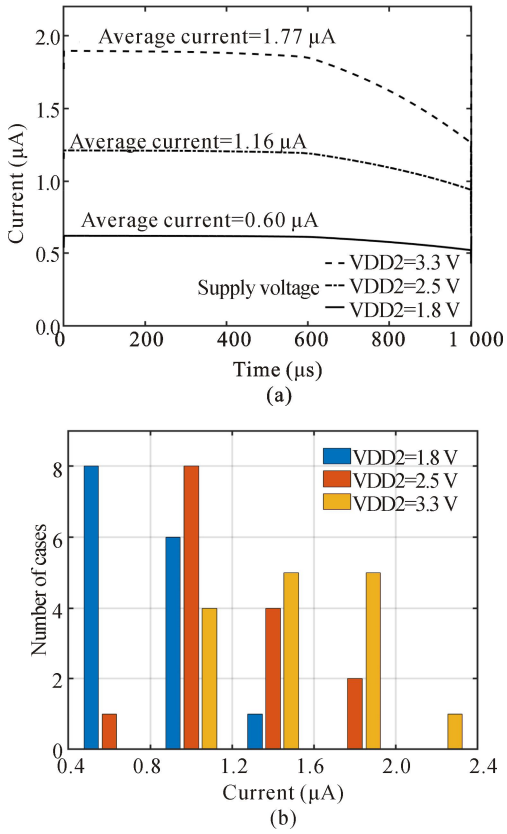


Fig.7 (a) Operating current of the feedback LOFIC pixel with supply voltage by VDD2 of 3.3 V, 2.5 V and 1.8 V; (b) Statistical results of PVT simulation

The current under different conditions can be counted by PVT simulation. Fig.7(b) presents the statistical results of 45 cases in which five process corners (tt, ss, sf, fs, ff), three temperatures (−40 °C, 27 °C, 80 °C) and three supply voltages (1.8 V, 2.5 V, 3.3 V) are selected. It can be demonstrated that when VDD2 is low, the number of cases is concentrated at the lower current. Then, the pixel performance after VDD2 reduction is reverified. The result shows that *FWC* is 75 ke- and *DR* is 101.9 dB, which is still better than the conventional LOFIC pixel. In addition, resolution reduction is also an effective method to further reduce the total power consumption for a large imager.

Fig.8 presents a series of specific layout designs under 110 nm CMOS process. Based on the addition of back-side-deep-trench-isolation (BDTI) layers between adjacent pixels in the array, the single pixel pitch is

5.0 μm×5.0 μm. Fig.8(a) shows the conventional LOFIC pixel layout designed with 13.3 fF capacitance, and Fig.8(b) presents the feedback LOFIC pixel layout designed with 13.3 fF capacitance. At the same time, to compare the capacitance area when realizing the same *DR*, the feedback LOFIC pixel layout of 7.0 fF capacitance is also designed, as shown in Fig.8(c). It should be noted here that the metal layers are used to form MIM capacitors. Therefore, the best exposure method is back-side-illuminated (BSI) design, that is, the light does not pass through the metal layers[16]. In this way, the space utilization of pixels can be improved without obstructing the normal path of PPD exposure and avoiding the decrease of fill factor and quantum efficiency.

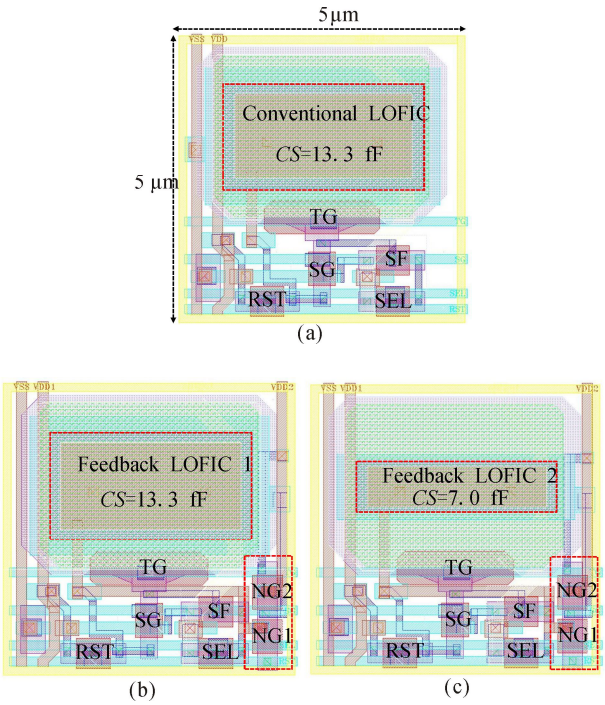


Fig.8 Pixel layouts design: (a) Conventional LOFIC with *CS*=13.3 fF; (b) Feedback LOFIC 1 with *CS*=13.3 fF; (c) Feedback LOFIC 2 with *CS*=7.0 fF

Tab.1 presents the specifications and performances of the above three pixels. It should be noted that the capacitance densities of different processes are quite different. In order to illustrate the benefit of feedback LOFIC, MIM capacitors based on the same process are uniformly used in the design here. By comparison, it can be confirmed that the proposed feedback LOFIC pixel can extend *FWC* from 44 ke- to 83 ke- and *DR* from 97.3 dB to 102.8 dB, although two transistors are added. Compared with the conventional LOFIC pixel, it reduces the dependence on capacitor area by 47% in the design of the same *DR*. In addition, it can also be further combined with the improved capacitance density method, which is suitable for the development trend of chip miniaturization and small pixel pitch.

Tab.1 Performances of the above three LOFIC pixels

	Feedback LOFIC 1	Feedback LOFIC 2	Conventional LOFIC
Process	110 nm	110 nm	110 nm
Pixel pitch	5.0 μm	5.0 μm	5.0 μm
CS	13.3 fF	7.0 fF	13.3 fF
CS compression	/	47 %	/
FWC	83 ke-	44 ke-	44 ke-
DR	102.8 dB	97.3 dB	97.3 dB
DR extension	5.5 dB	/	/
Setting time	75 ps	70 ps	25 ps
Operating current (VDD2=3.3 V)	1.77 μA	1.74 μA	/
(VDD2=1.8 V)	0.60 μA	0.58 μA	/

In this letter, a novel *HDR* pixel based on LOFIC and feedback structure is proposed. The feedback mechanism reduces the voltage drop of high light signal, thereby extending the detectable exposure range. The proposed feedback LOFIC pixel not only improves *FWC* and *DR* performances, but also means that when achieving the same *DR*, the capacitor area used is smaller than that of conventional LOFIC pixel. Although it adds a branch current, it provides a design reference to optimize *DR* and pixel pitch. This *HDR* pixel is conducive to adapting to the development trend of CMOS image sensors and their pixels miniaturization.

Ethics declarations

Conflicts of interest

The authors declare no conflict of interest.

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